What is claimed is:

1. A semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the memory cell matrix comprising:

a plurality device isolation films running along the column direction, arranged alternatively between the cell columns;

a plurality of first conductive layers arranged along the row and column-directions, a group of the first conductive layers arranged along one of column-direction is assigned to a corresponding cell column, adjacent groups of the first conductive layers are isolated from each other by the device isolation film disposed between the adjacent groups;

a plurality of lower inter-electrode dielectrics arranged respectively on crests of the corresponding first conductive layers, each of the lower inter-electrode dielectrics is made of insulating material containing at least silicon and nitrogen;

an upper inter-electrode dielectric arranged both on the device isolation films and the lower inter-electrode dielectric so that the upper inter-electrode dielectric can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns, the upper inter-electrode dielectric is made of insulating material different from the lower inter-electrode dielectrics; and

a plurality of second conductive layers running along the row-direction, each of the second conductive layers arranged on the upper inter-electrode dielectric so that the second conductive layer can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns.

2. The semiconductor memory of claim 1, further comprising a plurality of word lines running along the row-direction, each of the word lines is electrically connected to corresponding one of the second conductive layers.

3. The semiconductor memory of claim 2, further comprising a plurality of bit lines running along the column-direction, each of the word lines is shared by corresponding one of the cell columns.

4. The semiconductor memory of claim 3, further comprising:

a plurality of select transistors assigned respectively to end portions of corresponding cell columns; and

a select gate line electrically connected to gates of the select transistors.

5. The semiconductor memory of claim 1, wherein each of the lower inter-electrode dielectrics extends from the crest to the side surface of the first conductive layer so that a farthest end of the extending lower inter-electrode dielectric is sandwiched between the side surface of the first conductive layer and a side surface of corresponding device isolation film.

6. The semiconductor memory of claim 1, wherein each of the lower inter-electrode dielectrics is silicon

nitride film containing other elements than silicon and nitrogen less than approximately 20%.

7. The semiconductor memory of claim 1, wherein each of the upper inter-electrode dielectrics is a single layer film selected from the group consisting of an aluminum oxide film, a hafnium oxide film and a zirconium oxide film or a composite film including at least one of the single layer film.

8. A method for manufacturing a semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the method comprising:

forming a cell site gate insulator on a surface of a semiconductor substrate;

forming a first conductive layer on a surface of the cell site gate insulator;

selectively etching the first conductive layer, the cell site gate insulator and an upper portion of the semiconductor substrate so as to form a plurality of device isolation grooves running along the column direction, defining a plurality of ridges arranged alternatively between the device isolation grooves, each

of the ridges made of the first conductive layer, the cell site gate insulator and the upper portion of the semiconductor substrate;

filling a plurality of device isolation films in the device isolation grooves so as to isolate electrically the cell columns;

forming a plurality of lower inter-electrode dielectrics on the corresponding first conductive layers so that each of the lower inter-electrode dielectrics is isolated from other lower inter-electrode dielectrics belonging to other cell columns, each of the lower inter-electrode dielectrics is made of insulating material containing at least silicon and nitrogen;

forming an upper inter-electrode dielectric arranged both on the device isolation films and the lower inter-electrode dielectric so that the upper inter-electrode dielectric can be shared by different cell columns, the upper inter-electrode dielectric is made of insulating material different from the lower inter-electrode dielectrics; and

forming a second conductive layers on the upper inter-electrode dielectric.

9. The method of claim 8, wherein the forming lower inter-electrode dielectrics comprises:

removing natural oxide films formed on surfaces of the first conductive layers by gas etching in a CVD furnace; and

forming selectively the lower inter-electrode dielectrics on the surface of the first conductive layers in the CVD furnace, keeping the natural oxide removed surface of the first conductive layers airtight.

10. The method of claim 9, wherein the forming selectively the lower inter-electrode dielectrics is executed at substrate temperatures between 500° C to 700° C.

11. The method of claim 10, wherein the forming selectively the lower inter-electrode dielectrics is executed by CVD process using silicon halide as a source gas.

12. The method of claim 11, wherein the silicon halide is a chloride compound.

13. The method of claim 12, wherein the chloride compound is a compound selected from the group consisting of tetrachlorosilane and trichlorosilane.

14. The method of claim 9, wherein the removing natural oxide films is executed at substrate temperatures between 500° C to 900° C in hydrogen ambient.

15. The method of claim 9, wherein the removing natural oxide films is executed at reduced pressure.

16. The method of claim 8, wherein the forming lower inter-electrode dielectrics is executed by radical nitridation using nitrogen radicals.

17. The method of claim 8, wherein the forming lower inter-electrode dielectrics comprises:

annealing the surface of the first conductive layers under a nitric oxide gas ambient so as to form selectively the lower inter-electrode dielectrics on the surface of the first conductive layers and a silicon oxide film on the lower inter-electrode dielectrics; and

removing the silicon oxide film on the lower inter-electrode dielectrics.

18. The method of claim 8, wherein each of the lower inter-electrode dielectrics is silicon nitride film containing other elements than silicon and nitrogen less than approximately 20%.

19. The method of claim 8, wherein the upper inter-electrode dielectrics is a single layer film selected from the group consisting of an aluminum oxide film, a hafnium oxide film and a zirconium oxide film or a composite film including at least one of the single layer film.